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# LTSPICE MANUAL

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For Teaching Module EE4415

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## 1. Introduction

This manual is for users who are interested in using LTspice to simulate digital circuit. It focuses on DC and transient simulations. The manual describes how to find the delay, rise time and fall time in both methods – capture from waveform viewer and using MEASURE command. Power consumption simulation, static and dynamic power consumption, is stated as well.

The sample circuit used in the manual is an inverter. However, the methods presented in the manual can be applied to other digital circuit simulations.

### 1.1 Installation


You need to install LTspice and technology library to proceed. Follow the steps listed below to finish the installation.

- A. Download LTspice from <http://www.linear.com/designtools/software/> .
- B. Install LTspice following the prompts.
- C. Put the **CMOS\_018.lib** in **C:\Program Files\LTC\LTspiceIV\lib\sub** which is the default installation path (check yours if you didn't use the default installation path).
- D. Put **nmos\_018.asy** and **pmos\_018.asy** in **C:\Program Files\LTC\LTspiceIV\lib\sym** which is the default installation path (check yours if you didn't use the default installation path).

Both the LTspice and technology library have been installed if you have finished the steps above.

### 1.2 Schematic window

Schematic window is the window where you create schematic, specify simulation, edit command, and run simulation.

To open a schematic window, double click **LTSpiceIV** icon on the desktop (LTspice starts as Figure 1), and then click  on the LTspice window , an empty schematic window appears as Figure 2, where Draft1 is the default schematic name and .asc is LTspice extension of schematic.

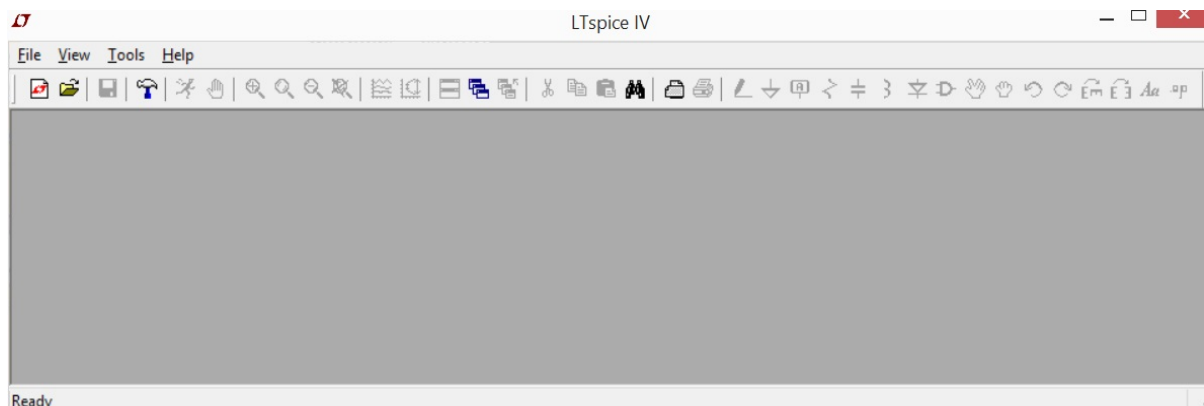


Figure 1. LTspice window

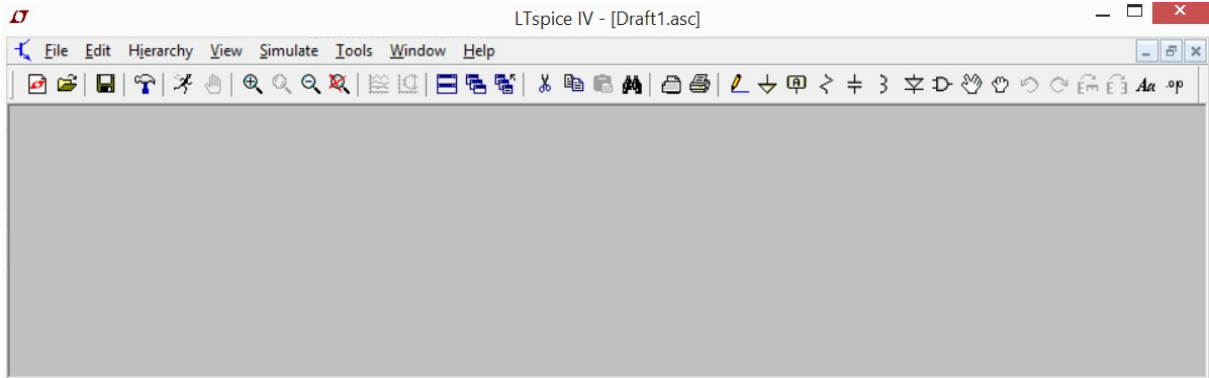


Figure 2. Schematic window

Moving mouse over the icon bar or click the menu on the tool bar, to see what functions they can perform.

### 1.3 Waveform viewer

The waveform viewer is the window where you can explore simulation results.

After each simulation, a waveform viewer (window) will automatically pop up with its name same as the schematic's name, as shown in Figure 3.

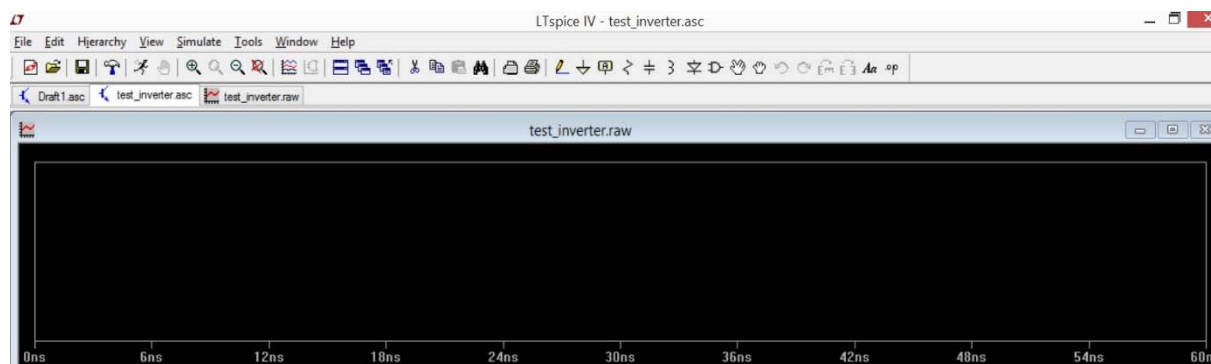


Figure 3. Waveform window

To plot the signals after simulation, do as follows:

- Left click on any wire to plot the voltage on the waveform viewer



- Left click on the body of the component to plot the current on the waveform viewer




Alternately, you can right click on the waveform window, and select **add trace** from the list to add signals from the available data field.

## 2. Creating Hierarchical Design

This chapter will show how to create a schematic, a symbol of the schematic, and a test bench of the schematic.

### 2.1 Creating a schematic

Following the steps listed below, to create a schematic.

- A. Open a schematic window as stated in section 1.2.
- B. Click  on the schematic window to add instances. The **Select Component Symbol** form pops up as Figure 4. It lists all the available symbols, including LTspice default symbols as well as the symbols installed in section 1.1.

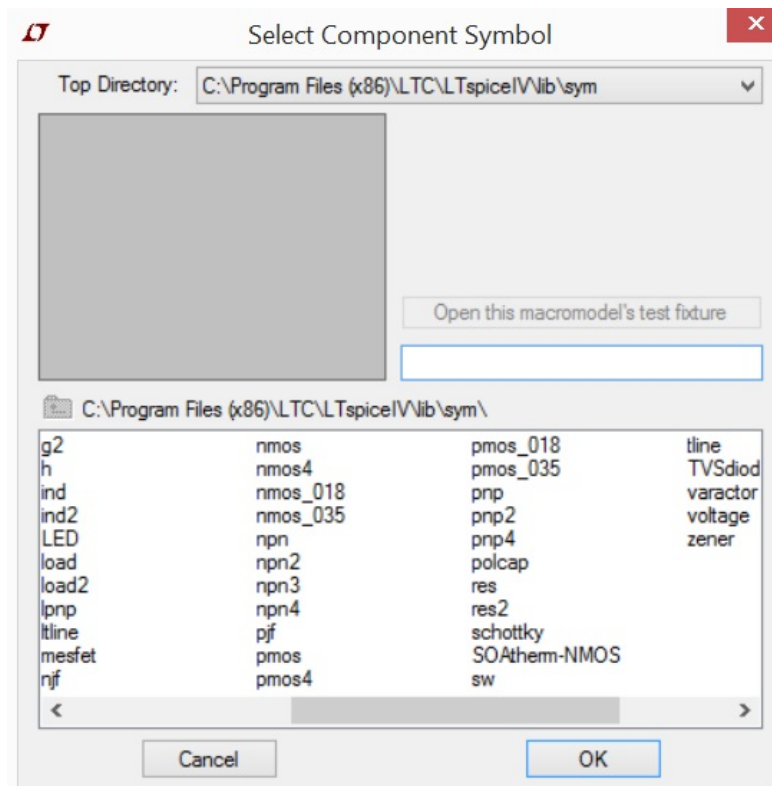



Figure 4. Select component symbol form

- C. Select **pmos\_018**, click **Ok** on the Select Component Symbol form, and then **click on the schematic window** to add pmos\_018.
- D. Repeat the procedure of step C to add **nmos\_018**.
- E. Press **Esc** to stop adding component.
- F. Click  on the schematic window to add ports. The **Net Name** form appears as Figure 5.

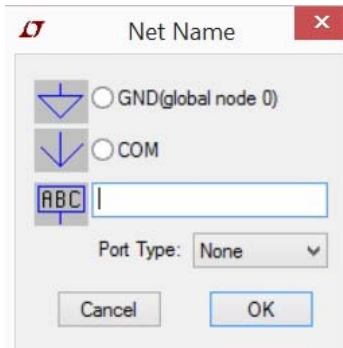


Figure 5. Net name form

- G. Enter **Vin** in the **ABC** field, choose **Input** for the **Port Type**, and then click **OK** on the Net Name form, and finally **click the schematic window** to add port Vin.
- H. Repeat the procedure of step G to add the following ports.

Port Name	Port Type
Vout	Output
VDD	Bi-Direct
GND	Bi-Direct

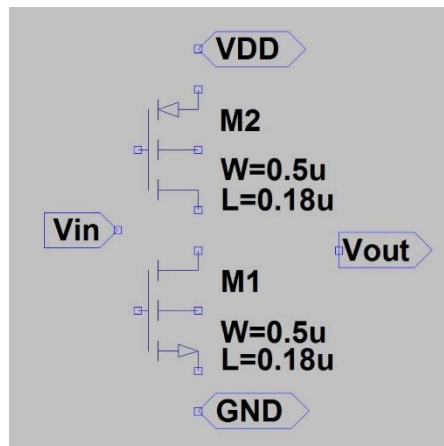
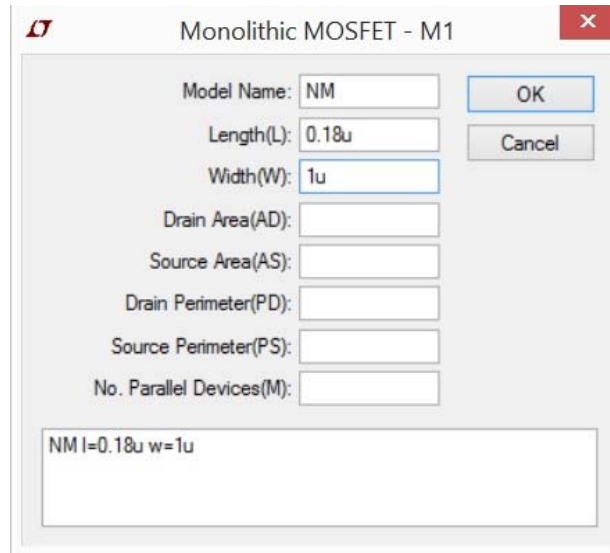


Figure 6. Schematic window with instances

- I. **Right click** the symbol if you need to change its size. A form with the symbol's property pops up. Change its **Width to 1u** as shown in Figure 7 and then click **OK** for the sample case. Keep AD, AS, PD, and PS unchanged, now, and these will be configured later, in step H.
- J. Repeat the step above to change the **width of pmos to 1u**, too.



Monolithic MOSFET - M1

Model Name: NM

Length(L): 0.18u

Width(W): 1u

Drain Area(AD):

Source Area(AS):

Drain Perimeter(PD):

Source Perimeter(PS):

No. Parallel Devices(M):

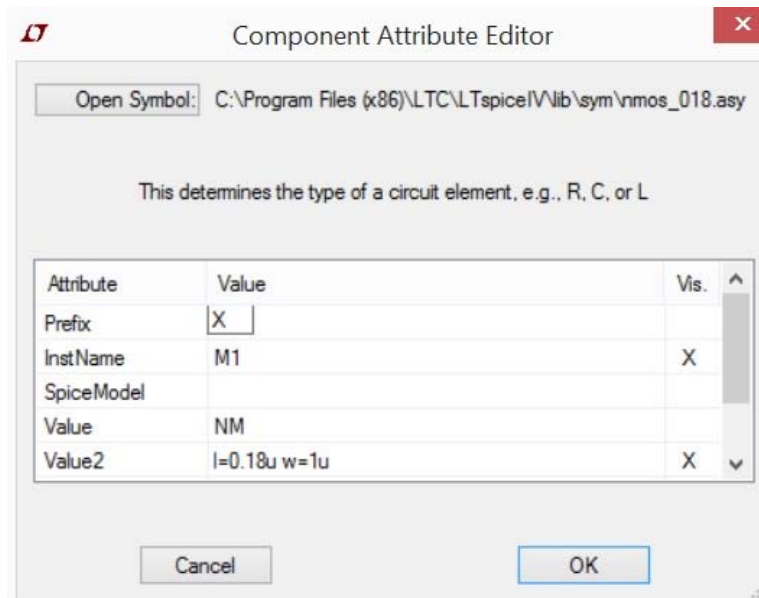
OK

Cancel

NM l=0.18u w=1u

Figure 7. NMOS property form

- K. **Hold Ctrl + right click** a mos symbol (example: nmos symbol) to configure AS, AD, PS and PD to use the sub circuit model included in the CMOS\_018.lib . On the Component Attribute Editor form, change **NM** to **X** on the row **Prefix** as Figure 8, and then click **OK** to finish it.



Component Attribute Editor

Open Symbol: C:\Program Files (x86)\LTC\LTspiceIV\lib\sym\nmos\_018.asy





This determines the type of a circuit element, e.g., R, C, or L

Attribute	Value	Vis.
Prefix	X	
InstName	M1	X
SpiceModel		
Value	NM	
Value2	l=0.18u w=1u	X

Cancel

OK

Figure 8. Component attribute editor

- L. Repeat the step above for the pmos symbol.
- M. Click  on the schematic window to wire the components. The circuit will look like Figure 9 after wiring. You can click  and then a symbol to move it, followed by click  or  to rotate or mirror it if necessary.

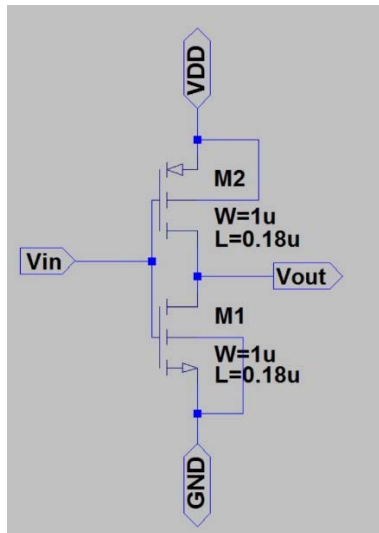



Figure 9. Schematic of inverter

N. Click **File** → **Save As** to save the schematic as **inverter.asc**.

## 2.2 Creating a symbol

The schematic has been created successfully. Next, it is to create a symbol for the schematic, so it can be used in hierarchical designs like invoking an nmos symbol when patching the inverter schematic. To create the symbol, following the steps stated below.

- Open the schematic window with click . Enter **inverter.asc** in the **File name** field for the sample case.
- Click **File** → **New Symbol** on the schematic window (inverter.asc window for the sample). A blank symbol window appears.
- Draw the symbol with lines, rectangles, circles, and etc from the pulldown menu – **Draw** as shown in Figure 10.



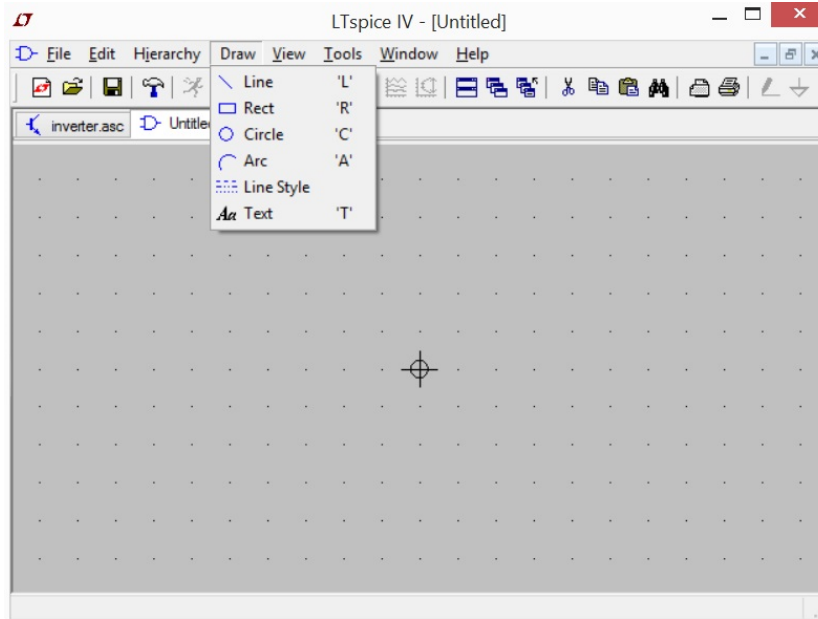


Figure 10. Symbol creation window

- D. The ports must be added as that of schematic (Figure 9 for the sample). Click **Edit → Add Pin/Port**. The Pin/Port Properties form displays as Figure 11, enter **Vin** in the **Label** field, and then tick **LEFT** under Pin Label Justification. Click **OK** and then the symbol window to add it.

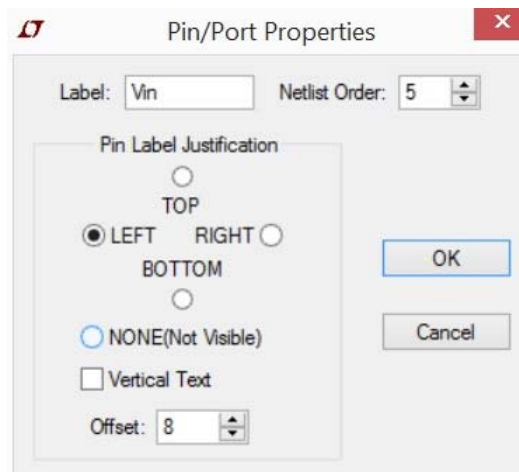


Figure 11. Add Pin/Port properties form

- E. Repeat step D to add the following ports. The symbol of the inverter schematic will be like Figure 12.

Port Name	Pin Label Justification
Vout	RIGHT
VDD	TOP
GND	BOTTOM

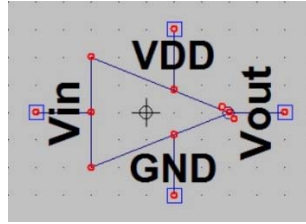




Figure 12. Symbol of the inverter

- F. Save the symbol after drawing with click **File → Save As...** . The name given must be **as same as the name of the schematic** and also it must be **saved in the same directory as that of the schematic**. For the sample case, it is saved as inverter.asy. Note that the extension of the symbol is **.asy** while the schematic is **.asc**.

Now, the symbol has been created and it is ready to be used for other designs.

## 2.3 Setup a test bench

A test bench is used to simulate a design (schematic) and check if it meets its design specifications. To setup a test bench, in fact, the processes are as same as creating a schematic described in section 2.1. Follow the steps listed below to setup the test bench of the inverter.

- A. Click  to open a new schematic window.
- B. Click  to add the self-created symbol (sample: inverter). **Enter the path** where you saved the symbol (inverter) in **Top Directory** field, choose the symbol, and then click **OK** as Figure 13.

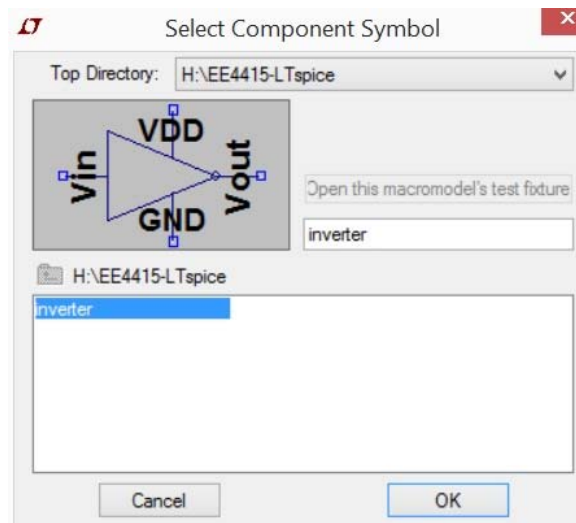


Figure 13. Add self-created symbol

- C. Click  to add LTspice symbols: one **cap** and two **voltage** as shown in Figure 14.

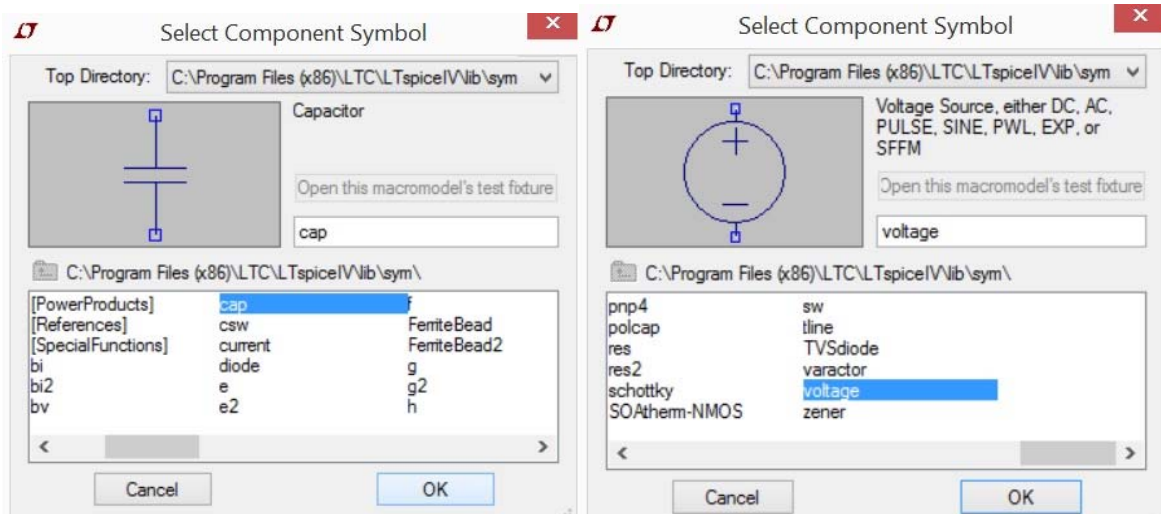



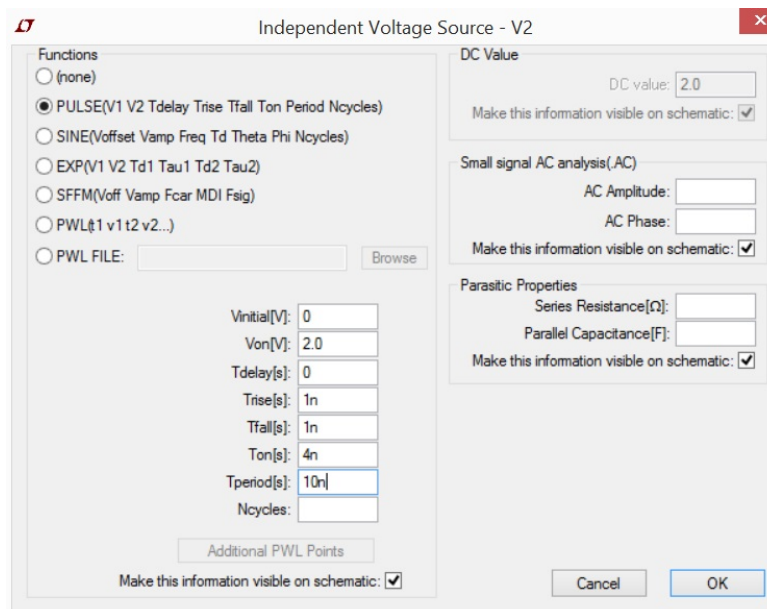
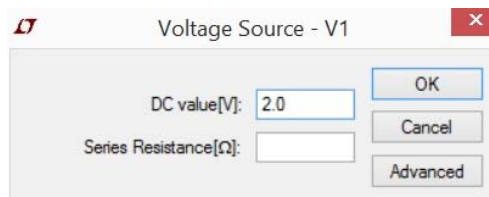


Figure 14. Add the symbols of cap and voltage

- D. Click  on the schematic window to add ground.
- E. Click  to add port **Vout** with the Port Type as **Output**.
- F. Click  to connect the symbols as Figure 16.
- G. Edit the properties of the components: V1 (DC source), V2 (Pulse), and C1 (capacitor) with right click each of them, referring to Figure 15.



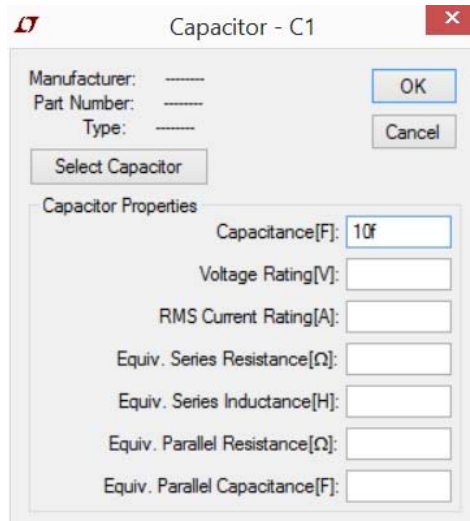
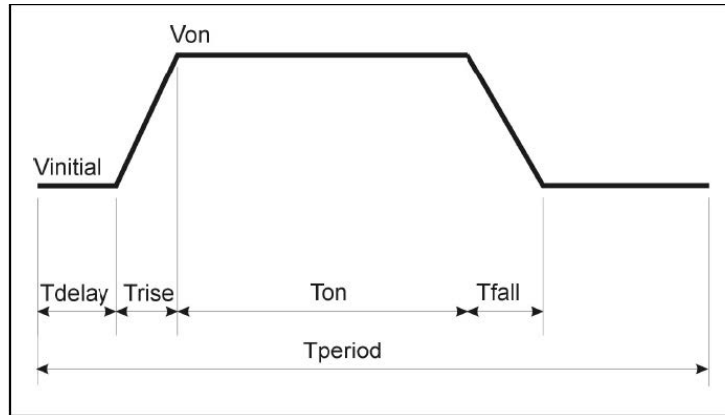


Figure 15. Edit properties of the components

H. Save the schematic.

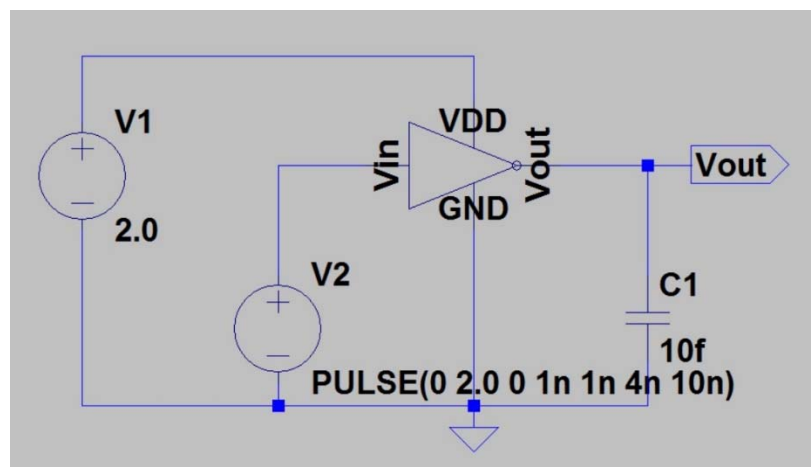




Figure 16. Test bench of the inverter

The test bench has been created as Figure 16.

### 3. DC Analysis

This chapter shows how to run DC analysis with the sample - inverter test bench, following the steps listed below.

- A. Click  to open the test bench which is created in section 2.3.
- B. To add wire names for viewing the results after simulation, click  to add **VDD** and **Vin** with **Port Type – none**, one by one with **click** the respective wires as Figure 17 shows.

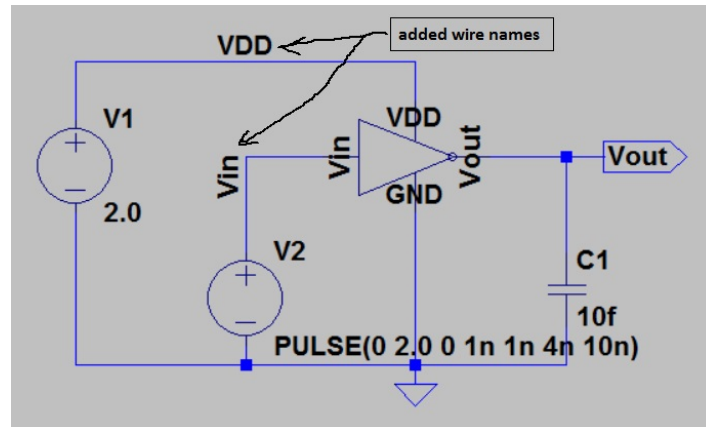



Figure 17. The test bench with wire names

- C. Click  to save the schematic.
- D. Click **Simulate → Edit Simulation Cmd.**
- E. Select the **DC sweep** tab on the Edit Simulation Command form, **enter** the fields under the 1<sup>st</sup> Source as Figure 18, click **OK** on the form, and then **click the schematic window** to put the command on the window.

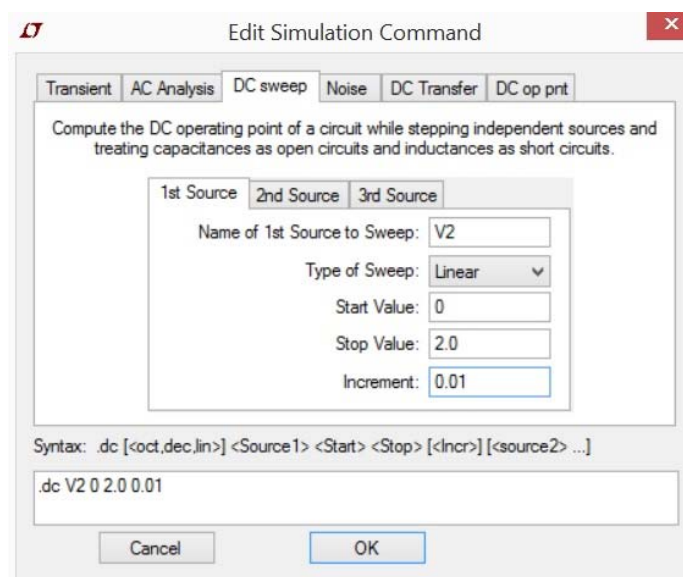


Figure 18. Edit simulation command

Note: Figure 18 shows that it will do DC analysis with sweep V2 from 0V to 2.0V in a step size of 0.01 volts.

- F. Click  to add SPICE directive. Enter **.lib CMOS\_018.lib** in the blank field as shown in Figure 19, click **OK** and then **click on the schematic window** to add it.

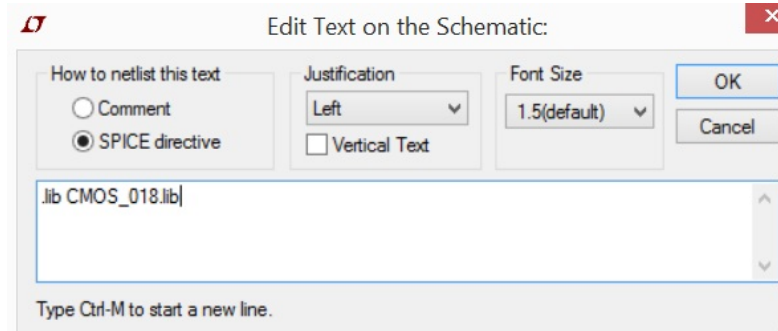



Figure 19. Add SPICE directive

**Note: CMOS\_018.lib is the user defined model library. Without adding it, the simulation cannot start.**

- G. Click  to start DC simulation. An empty waveform window appears automatically after the simulation is successfully finished. If there is problem with the simulation, you can get error information from **View → SPICE Error Log**.
- H. Move your mouse over to the schematic window, and then click the wires labeled with **Vin** and **Vout**. The waveforms of Vin and Vout display on the waveform viewer as shown in Figure 20.

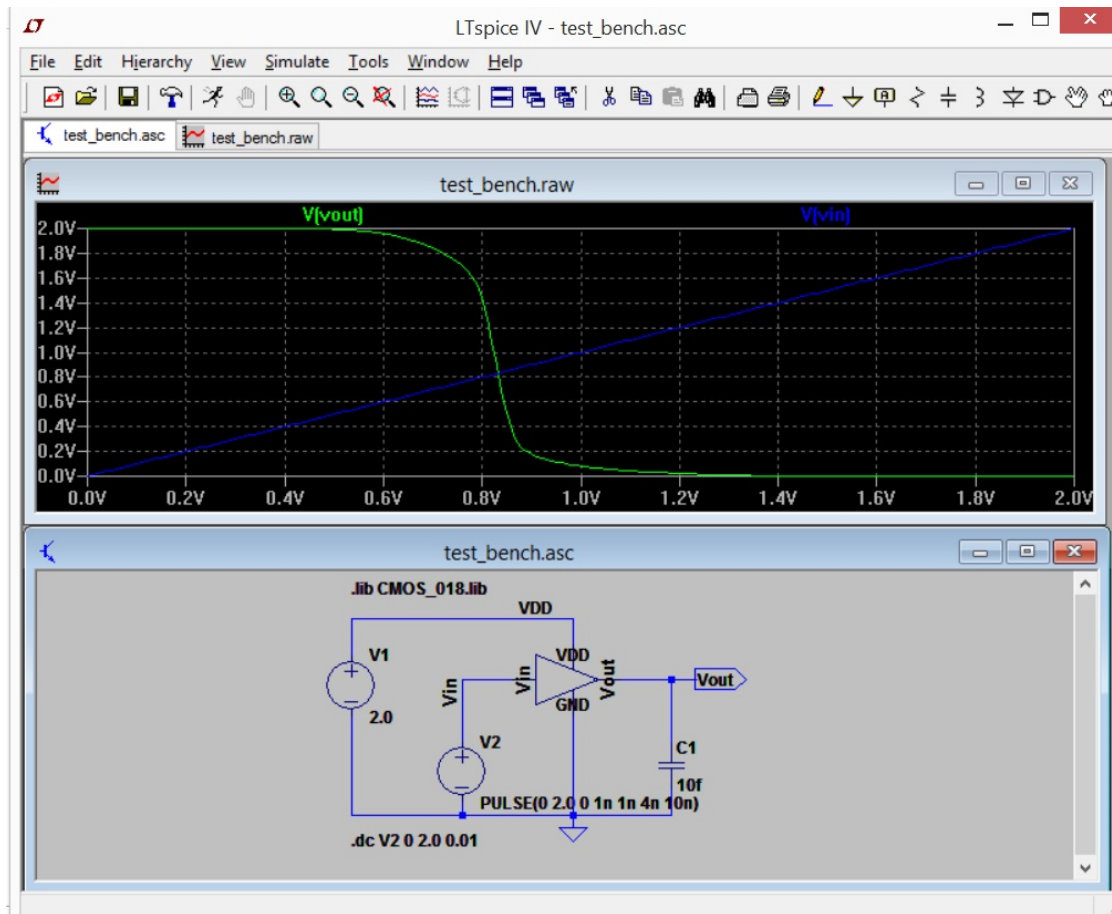



Figure 20. Waveforms and the test bench

- I. **Right click** your mouse on the waveform window, choose **Add Trace** to check other signals of the test bench.

Now, DC simulation is finished. Next Chapter, we will see how to do transient simulation.

## 4. Transient Analysis

This chapter describes how to run a transient analysis with LTspice. Following the steps listed below, using the sample circuit – test bench, go through the procedures of transient analysis.

- A. Click  to open the test bench which you used in section 3.
- B. Click **Simulate** → **Edit Simulation Cmd** to bring up the Edit Simulation Command form.
- C. Click the **Transient** tab on the form, and then enter **40n** in the field of **Stop Time** and **0.1n** in the field of **Time to Start Saving Data**, leaving others unchanged.
- D. Click **OK** on the form and then **click the schematic window** to insert the command. The Edit Simulation Command and the schematic are shown in Figure 21.



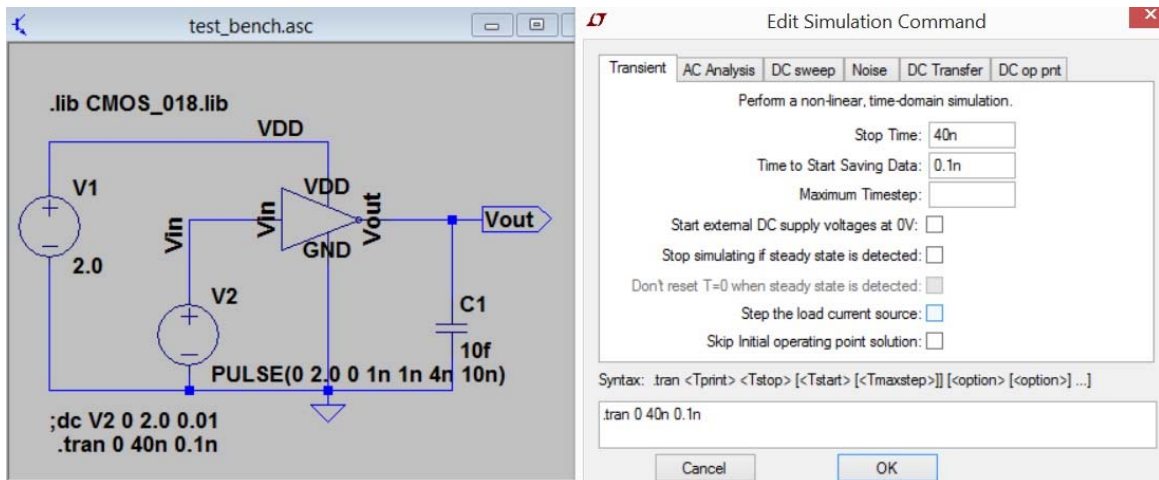



Figure 21. Command for transient simulation

Note: the semicolon in front of dc means the DC simulation is disabled.

- E. Click  to start transient simulation. If there is any problem with the simulation, you can get error information from View → SPICE Error Log.
- F. Move your mouse over to the schematic window, and then click the wires labeled with **Vin** and **Vout**. The waveforms of Vin and Vout display on the waveform viewer as shown in Figure 22.

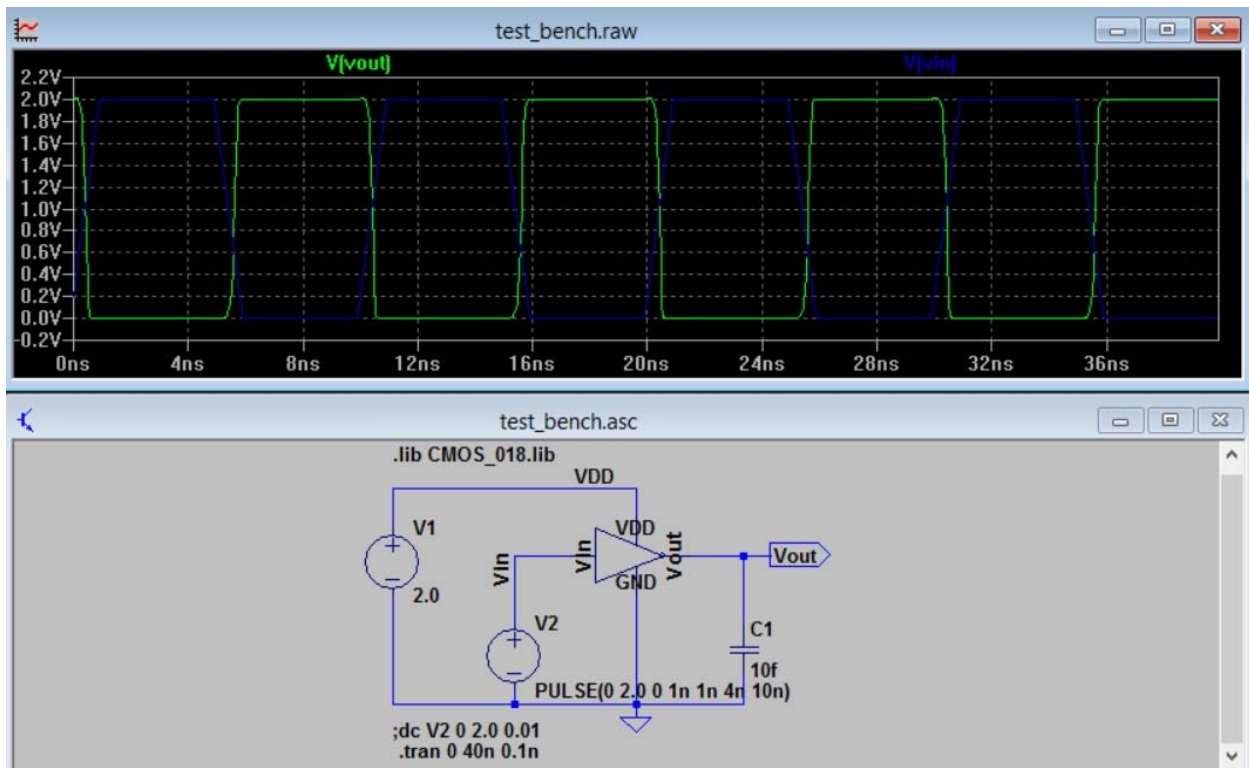


Figure 22. Waveforms of transient analysis for the test bench

Transient analysis is finished, up to now. Next, we will look into the waveforms of the transient simulation, to get the delay, rise time and fall time as well as the power consumption from the waveform viewer.



## 5. Delay Simulation

This chapter depicts how to find the delay of a circuit from the waveforms, and shows what **.MEAS** commands should be used to get the delay, with the same sample circuit – inverter.

### 5.1 Capture from waveforms

Follow the steps listed below to get the delay from waveforms.

- Click **Vout** and **Vin** to get the waveforms of the inverter after transient simulation.
- Click **the waveform window** to activate it.
- Click **Plot Setting → Add Trace**, enter **1** which equals to  $50\% \times V_{in}$  (or  $50\% \times V_{out}$  for this case) in the field of **Expressions(s) to add** of the Add Traces to Plot form, and then click **OK** on the form, as figure 23. A horizontal line with the value of 1V is added on the waveform window as shown in Figure 24.

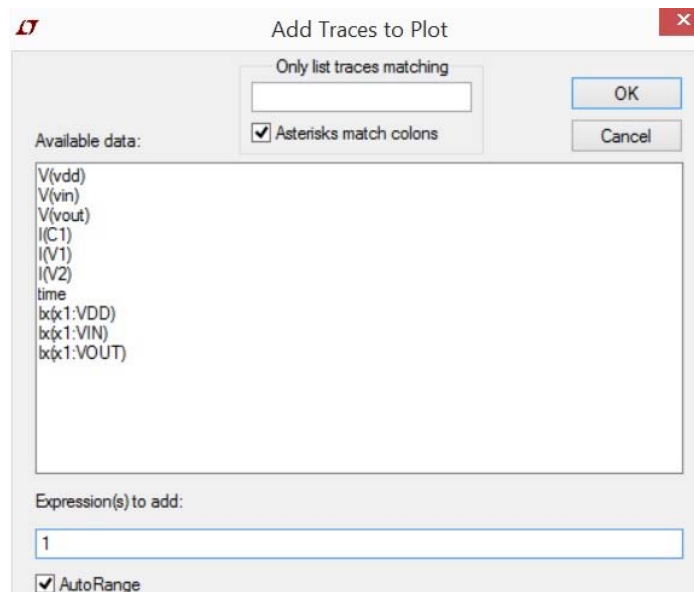


Figure 23. Add traces to plot window

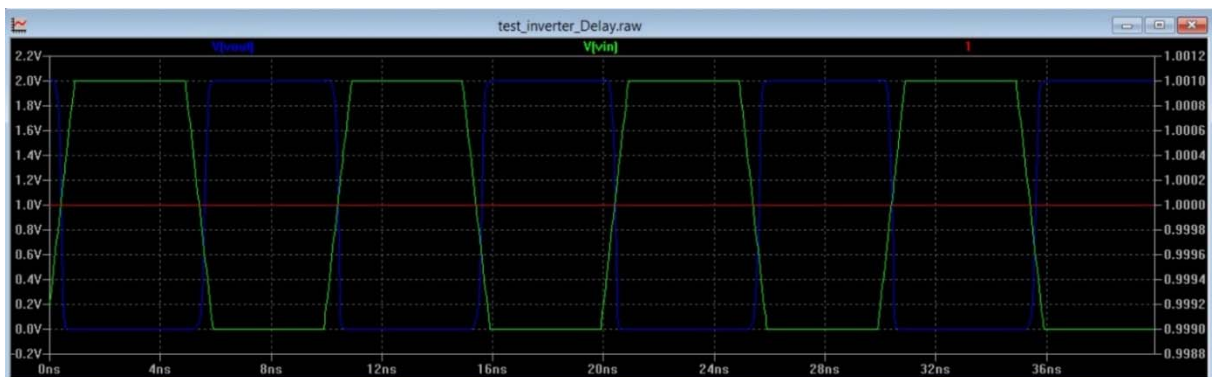



Figure 24. Waveforms of the inverter

- D. Click , and then **draw a rectangle** over the last cycle of the waveforms with holding the **left button** of the mouse to enlarge the area. Now, it looks like Figure 25. It could be zoomed in further if necessary, for viewing the  $t_{pHL}$  and  $t_{pLH}$  clearly.

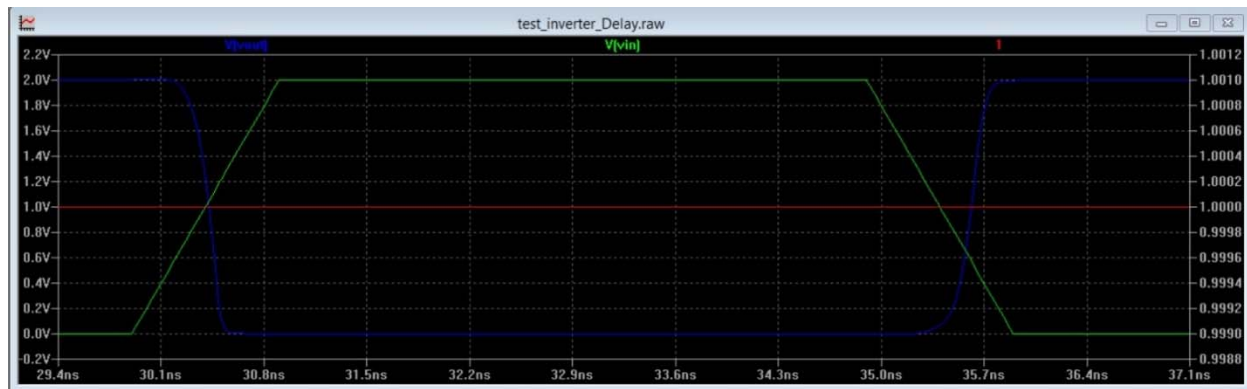


Figure 25. Waveforms after zoomed in

- E. Right click **V(vout)** label on the waveform window to add 1<sup>st</sup> and 2<sup>nd</sup> cursors as Figure 26.

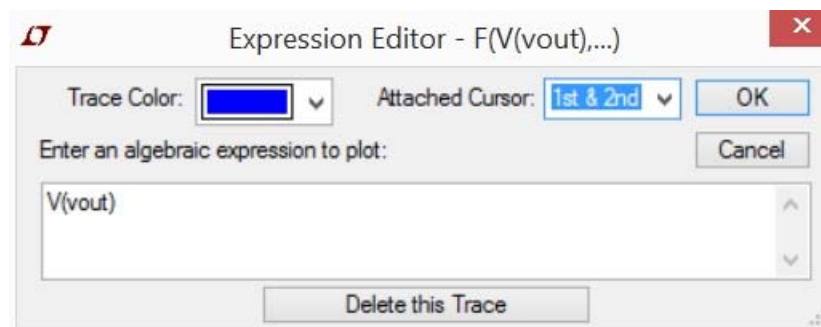


Figure 26. Add cursors

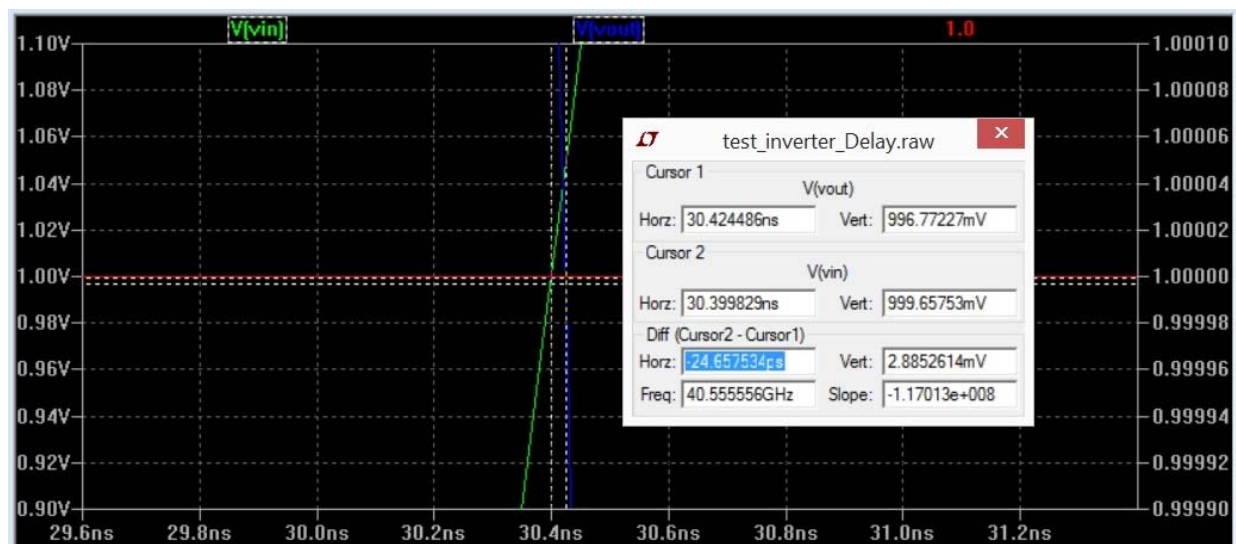


Figure 27. Find  $t_{pHL}$  from the graph



- F. Move the cursors and zoomed in further to find the  $t_{pHL}$ . It is equal to 24.657534ps as Figure 27 shows, which should equal to the absolute value of Diff (Cursor2 – Cursor1).
- G. Repeat step F to find  $t_{pLH}$ . It is 209.0268ps as Figure 28.



Figure 28. Find  $t_{pLH}$  from the graph

Now, the delay can be calculated with  $t_{\text{delay}} = 0.5 \times (t_{pHL} + t_{pLH}) = 116.842167\text{ps}$ . The value of the delay may not be accurate because it depends on the positions of the cursors being put.

## 5.2 Using .MEAS

- A. Click  to open the test bench
- B. Click  to add SPICE directive, and enter the .MEAS commands in the blank field as Figure 29.

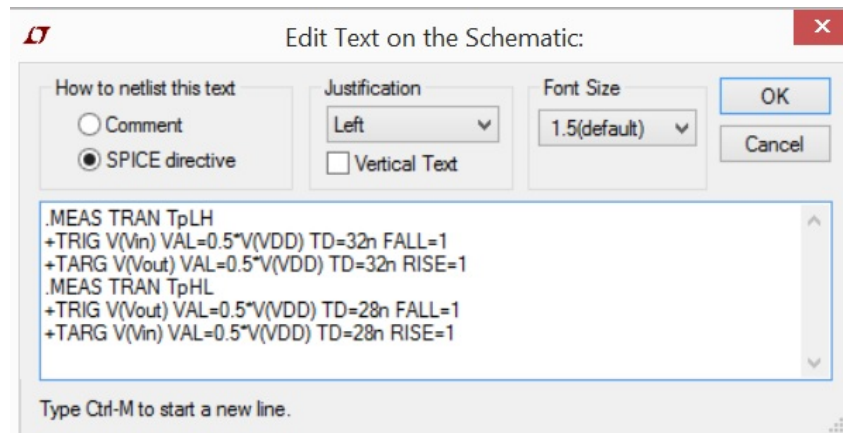


Figure 29. Commands for measuring the delay

Note: TD=32n FALL=1 (or RISE=1) means the first fall edge (or rise edge) after 32ns.

- C. Click **OK** on the **Edit Text on the Schematic** form, and then **click the schematic window** to insert it. The schematic looks like Figure 30, now.

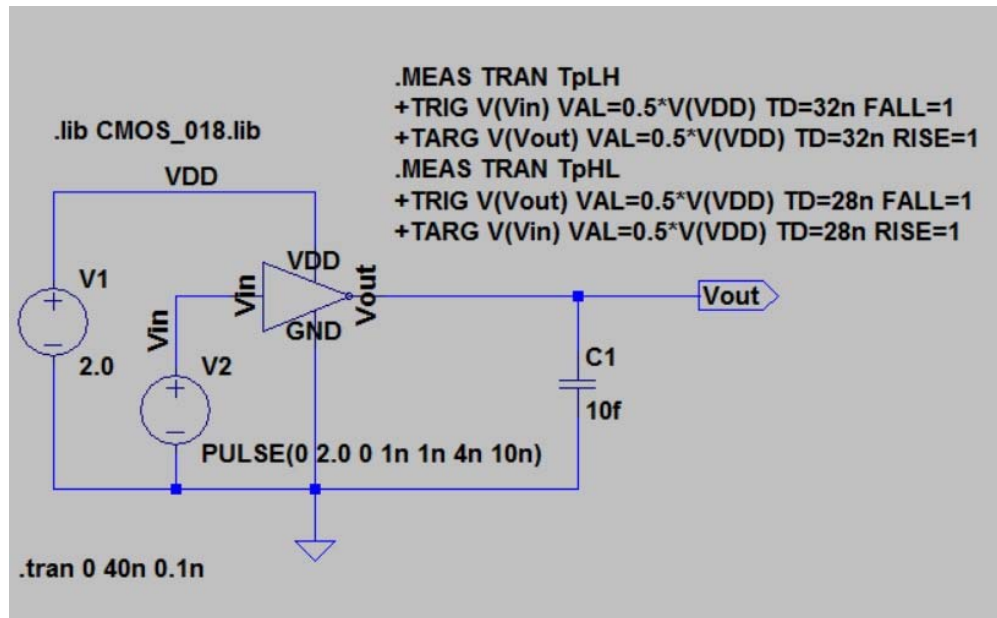


Figure 30. Test bench with the .MEAS commands for measuring delay

- D. Click  to run the transient simulation.
- E. When the simulation stops, Click **View** → **SPICE Error Log**. The **SPICE Error Log** window pops up as Figure 31. The t<sub>plH</sub> and t<sub>phL</sub> are shown and highlighted with the red rectangle in Figure 31.

```

SPICE Error Log: H:\EE4415-LTspice\test_inverter_Delay.log
Circuit: * H:\EE4415-LTspice\test_inverter_Delay.asc
Direct Newton iteration for .op point succeeded.
Ignoring empty pin current: Ix(x1:gnd)
Ignoring empty pin current: Ix(x1:gnd)
tplh=2.1054e-010 FROM 3.54e-008 TO 3.56105e-008
tphl=-2.41424e-011 FROM 3.04241e-008 TO 3.04e-008
Date: Tue Nov 15 14:18:55 2016
Total elapsed time: 0.218 seconds.
tnom = 27
temp = 27
method = modified trap
totiter = 2436
traniter = 2429
tranpoints = 1134
accept = 1110
rejected = 24
matrix size = 5
fillins = 0
solver = Normal
Matrix Compiler1: 132 bytes object code size 0.1/0.1/[0.1]
Matrix Compiler2: 28 opcodes 0.1/[0.1]/0.1

```

Figure 31. SPICE log with the delay information

The delay,  $t_{\text{delay}} = 0.5 \times (t_{\text{pHL}} + t_{\text{pLH}}) = 117.3412\text{ps}$ , which is more accurate. The values with both the methods are approximately same.

## 6. Rise Time and Fall Time

This chapter describes how to get the rise time and fall time of a circuit. As in chapter 5, both methods – capture from waveforms and using .MEAS command are discussed with the same test bench.

### 6.1 Capture from waveforms

- A. After the transient analysis, click the wire labeled with Vin and Vout on the schematic window.
- B. Click **Plot Setting** → **Add Trace**, add **0.2V** which equals to 10% x Vout and then click **OK**.
- C. Click **Plot Setting** → **Add Trace**, add **1.8V** which equals to 90% x Vout and then click **OK**. Now the waveform window looks like Figure 32.

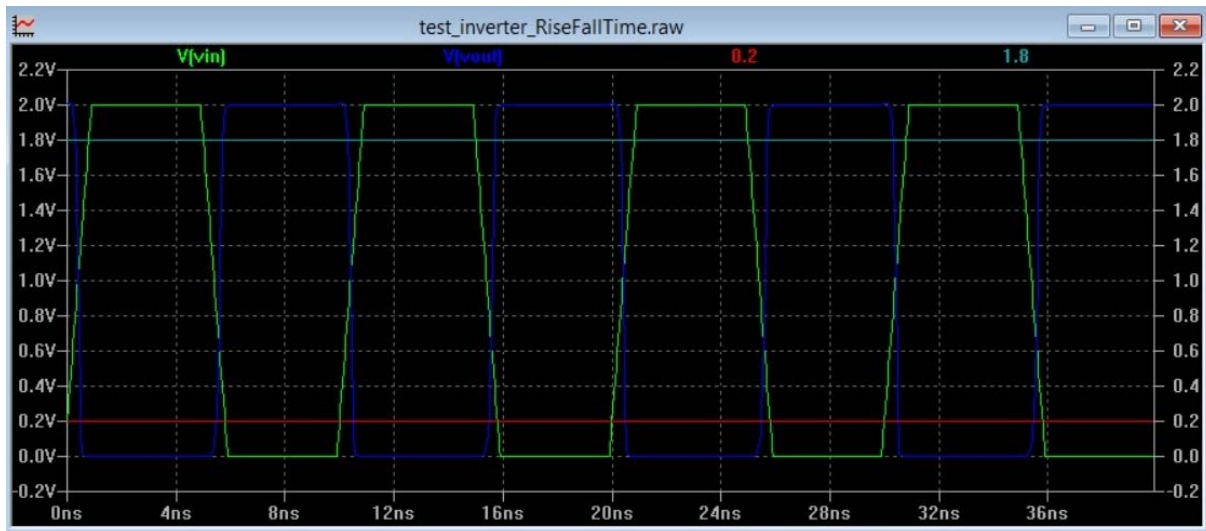


Figure 32. Waveforms with 10% x Vout and 90% x Vout

- D. **Right click** the **V(vout)** label on the waveform window to add the cursors as Figure 26.
- E. Move the cursors to the rising edge of the Vout to find the rise time as Figure 33. The rise time equals to 218.51852ps which is the absolute value of the Diff (Cursor2-Cursor1)



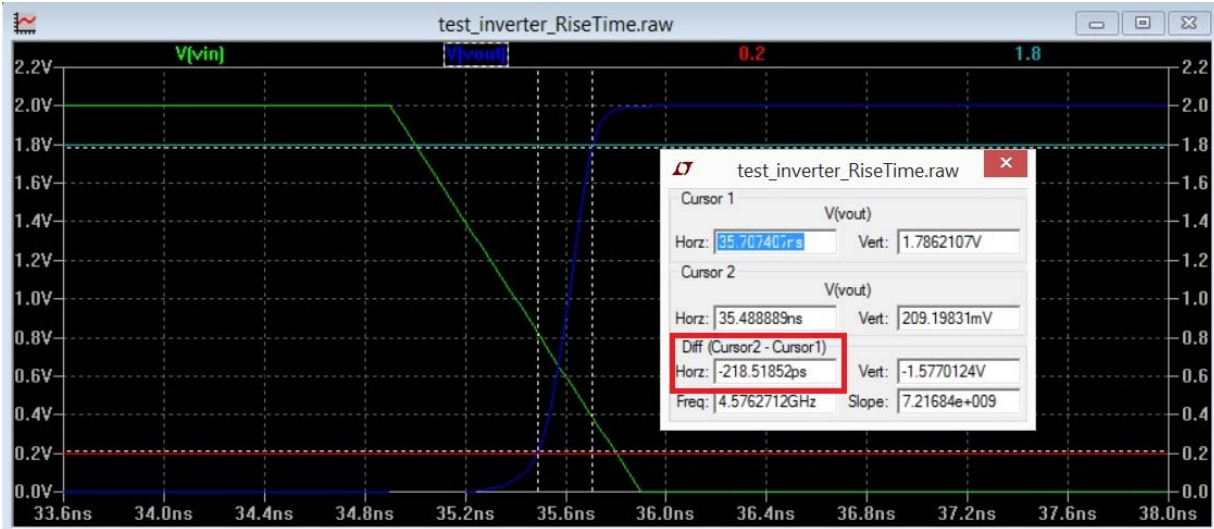


Figure 33. Capture the rise time from graph

- F. Then, move the courses to the falling edge of Vout to find the fall time as Figure 34. The fall time equals to 198ps.

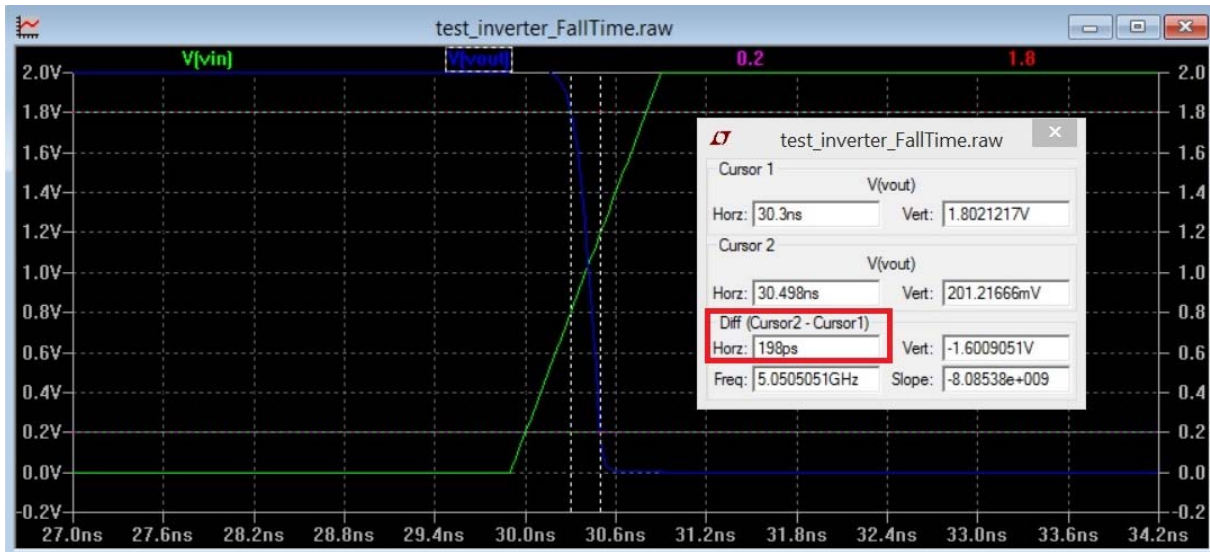


Figure 34. Capture the fall time from graph

## 6.2 Using .MEAS

To find the rise time and the fall time, simply repeat the steps listed in section 5.2 but replace the .MEAS commands with those shown in Figure 35. The rise time and fall time are equal to 225.269ps and 197.423ps respectively, referring to Figure 36.

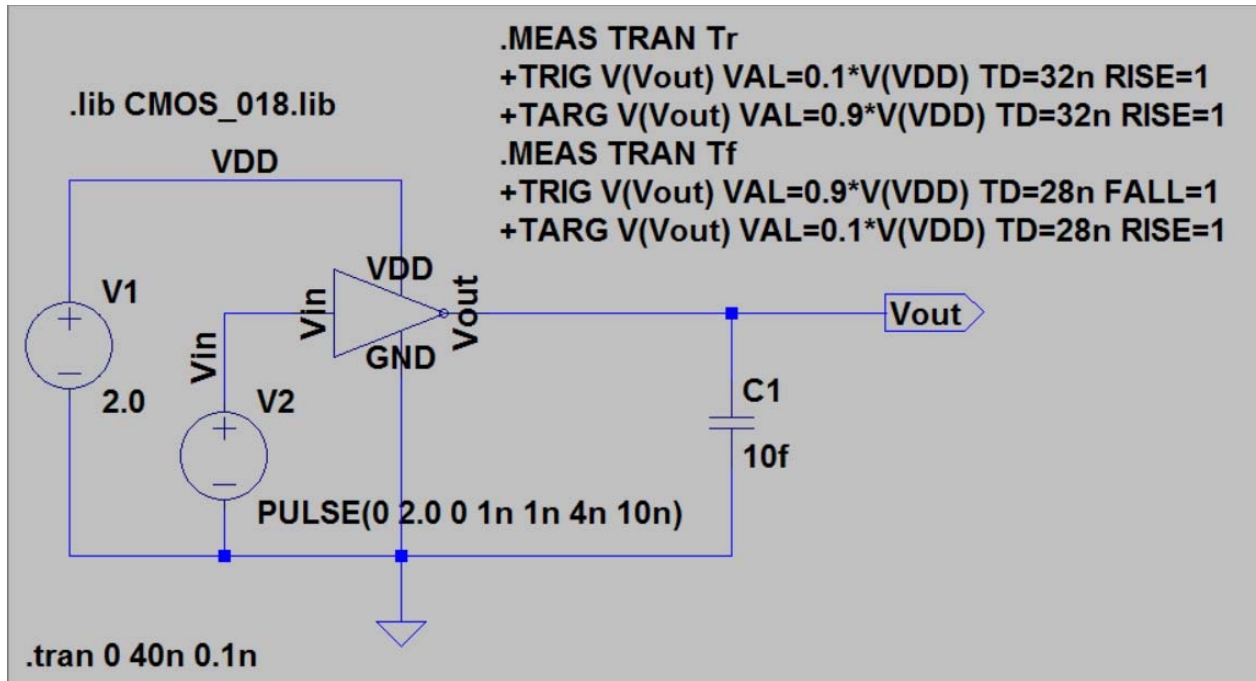


Figure 35. The test bench with the .MEAS commands for getting the rise time and fall time.

```

SPICE Error Log: H:\EE4415-LTspice\test_inverter_RiseFallTime.log
Circuit: * H:\EE4415-LTspice\test_inverter_RiseFallTime.asc
Direct Newton iteration for .op point succeeded.
Ignoring empty pin current: Ix(x1:gnd)
Ignoring empty pin current: Ix(x1:gnd)
tr=2.25269e-010 FROM 3.54853e-008 TO 3.57106e-008
tf=1.97423e-010 FROM 3.03007e-008 TO 3.04982e-008
Date: Wed Nov 02 15:03:53 2016
Total elapsed time: 0.151 seconds.
tnom = 27
temp = 27
method = modified trap
totiter = 2436
traniter = 2429
tranpoints = 1134
accept = 1110
rejected = 24
matrix size = 5
fillins = 0
solver = Normal
Matrix Compiler1: 8 opcodes 0.1/[0.1]/0.1
Matrix Compiler2: 335 bytes object code size 0.1/0.1/[0.1]

```

Figure 36. SPICE Log for viewing the rise time and fall time.

## 7. Power Consumption Simulation

This chapter shows how to get the power consumption with the two methods used in the previous chapters.

### 7.1 Static power

Following the steps below to find out the static power consumption.

- Open the test bench circuit.
- Connect **V2** to **ground**, and add **.MEAS** commands as Figure 37.

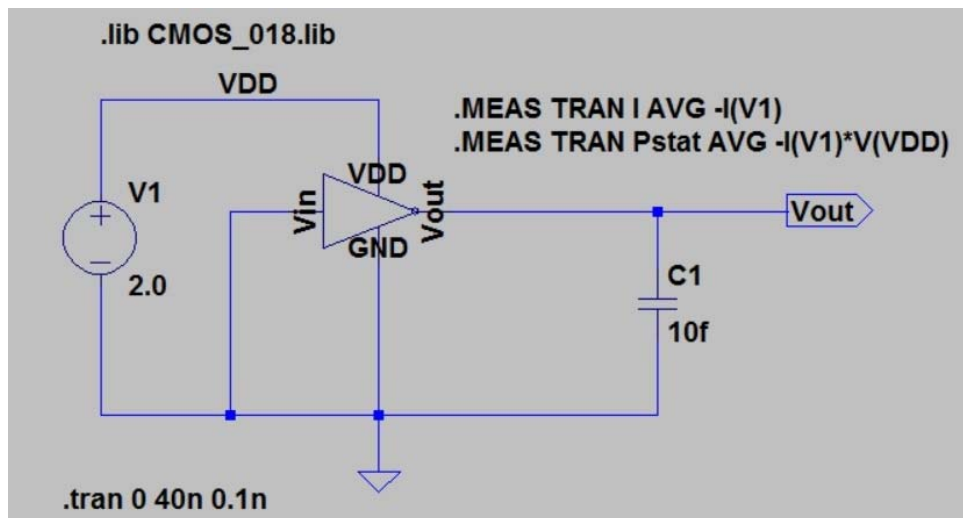


Figure 37. Test bench for static power consumption


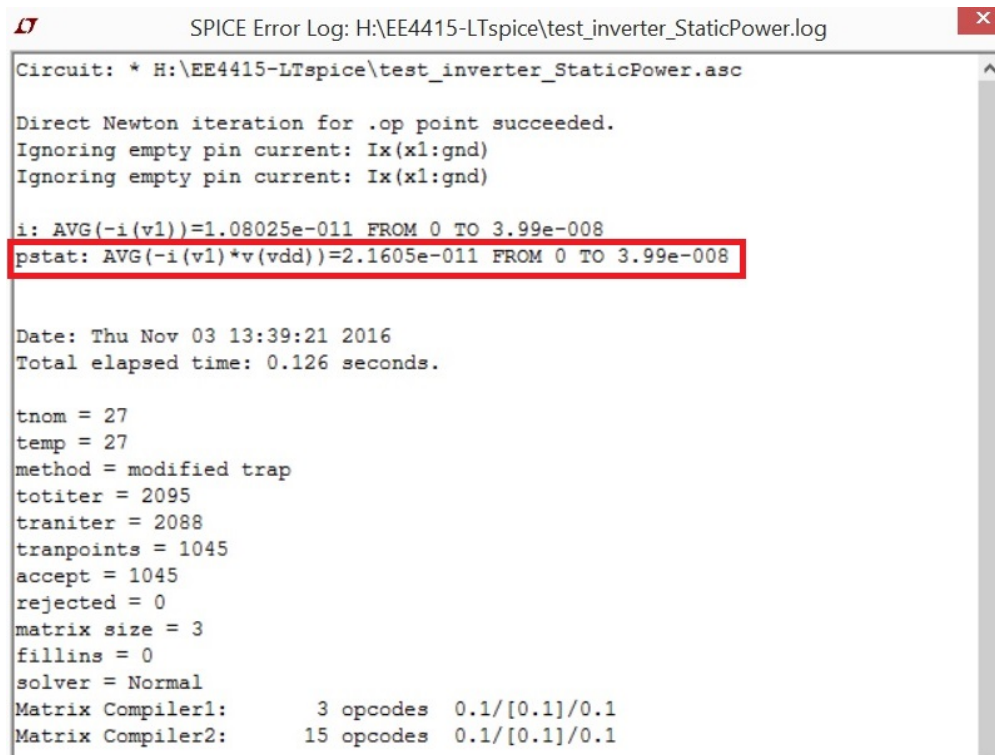
- Run the test bench with click .
- Add trace  $-I(V1)*V(vdd)$  on the waveform window with click **Plot Settings** → **Add trace**.
- Hold the **Ctrl** key + press **left mouse button** over the waveform label of  $-I(V1)*V(vdd)$ . A small table with the average power consumption pops up. The reading is 21.605pW.



Figure 38. Capture the static power from waveforms



- F. Open the SPICE Error Log window, the average power (pstat) also can be found, which is  $2.1605e-011$



```
SPICE Error Log: H:\EE4415-LTspice\test_inverter_StaticPower.log

Circuit: * H:\EE4415-LTspice\test_inverter_StaticPower.asc

Direct Newton iteration for .op point succeeded.
Ignoring empty pin current: Ix(x1:gnd)
Ignoring empty pin current: Ix(x1:gnd)

i: AVG(-i(v1))=1.08025e-011 FROM 0 TO 3.99e-008
pstat: AVG(-i(v1)*v(vdd))=2.1605e-011 FROM 0 TO 3.99e-008

Date: Thu Nov 03 13:39:21 2016
Total elapsed time: 0.126 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2095
traniter = 2088
tranpoints = 1045
accept = 1045
rejected = 0
matrix size = 3
fillins = 0
solver = Normal
Matrix Compiler1:      3 opcodes  0.1/[0.1]/0.1
Matrix Compiler2:     15 opcodes  0.1/[0.1]/0.1
```

Figure 39. Static power consumption with .MEAS

## 7.2 Dynamic power

The method to find the average dynamic power is as same as that to find the average static power, except that V2 is connected back to the pulse as Figure 40.

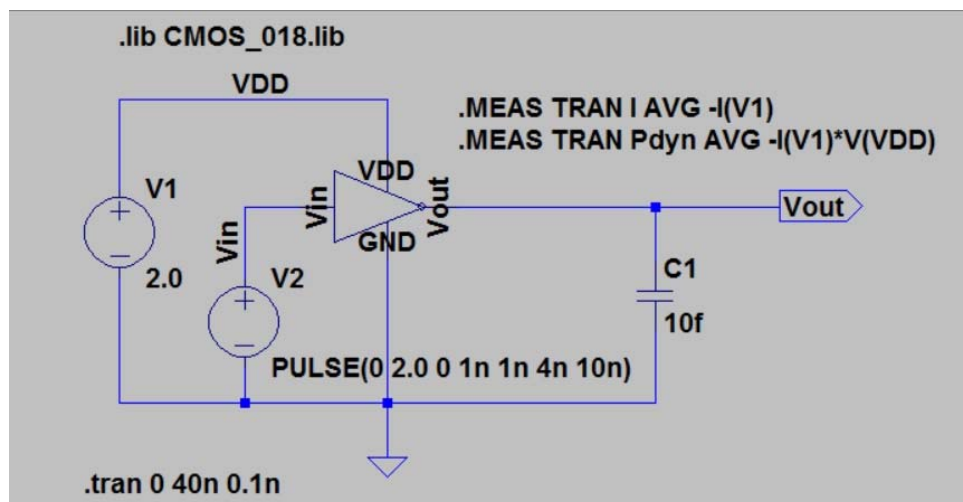


Figure 40. Test bench for the dynamic power consumption

After simulation, view the SPICE Error Log to find the average power consumption as Figure 41. It also can be found from the waveform viewer as Figure 42.

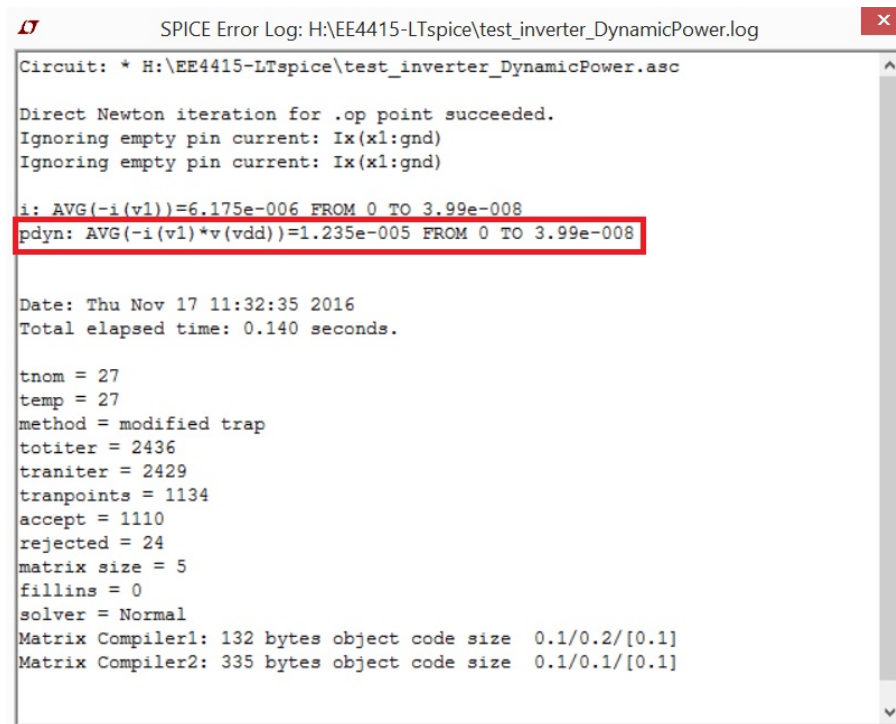


Figure 41. Dynamic power consumption with .MEAS

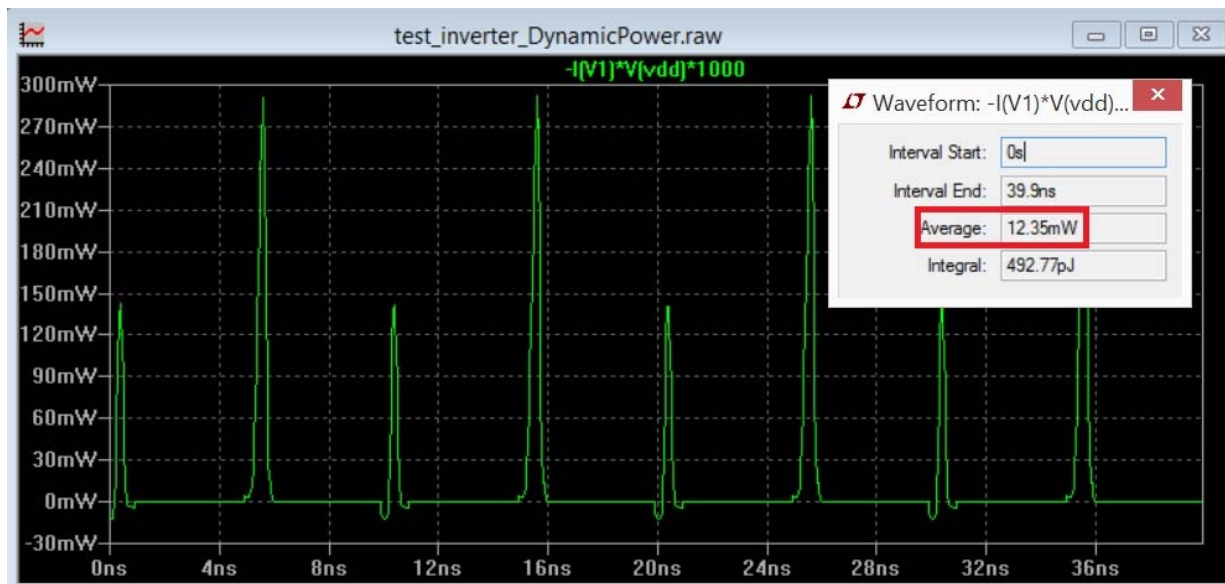


Figure 42. Capture the dynamic power from waveforms

## 8. Conclusion

The manual describes how to run DC and transient simulations with LTspice. It also elaborates how to find the delay, rise time, fall time, and average static power consumption as well as the average dynamic power consumption. Two methods are used in the elaboration, capture from waveforms and using spice measure command.

Thanks for using the manual. You are welcome to feedback.